

# An Experimental Verification of a Simple Distributed Model of MIM Capacitors for MMIC Applications

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**Abstract**—A distributed model has been derived for MIM capacitors using a simple coupled-transmission-line approach. The model has been compared with measured *S*-parameter data from MIM capacitors having different aspect ratios fabricated on 4-mil GaAs substrates. The agreement is very good. The derived model will converge to the first-order capacitor model, generally given in the literature, under a few assumptions.

## I. INTRODUCTION

EXTENSIVE USE is being made of MIM (metal-insulator-metal) capacitors in MMIC technology, both as tuning and as RF bypass elements. It is important to predict the performance of such capacitors in terms of their losses and behavior as lumped elements. The losses in the capacitors used as tuning and dc-blocking elements in high-power applications may be very damaging. The metallic losses and the dielectric material losses in a MIM capacitor determine the overall quality factor  $Q$  of the capacitor. In the present model, the metal loss will be included in the form of skin losses and the dielectric loss in the form of loss tangent. The loss tangent of the dielectric was maintained constant over the measurement frequency range, because this gave a better fit to the measured *S*-parameter data. With the dielectric loss tangent dominating the capacitor quality factor, the overall quality factor of the capacitor in our case shows a tendency to decrease with frequency due to the additional metal plate losses, which increase with frequency.

In the literature, there have been a number of publications on the approximate model of such capacitors [1], [2]. In most practical applications, the approximate model may be adequate if (i) the substrate effects can be neglected, (ii) the capacitor dimensions are much smaller than the propagating wavelength, and (iii) the losses due to metal plates are very small [3]. In [3], the author did not consider the mutual inductive coupling between the capacitor plates.

This paper presents a distributed model based on a coupled-transmission-line approach. In order to make a comparison with the calculated values, the element values of the model have been optimized to fit the measured

two-port *S*-parameters of the capacitors with different aspect ratios and different values. A constrained optimization routine has been written for this purpose to implement the fitting with a high degree of accuracy.

## II. MODELING

The MIM capacitor (Fig. 1) can be represented by a pair of coupled transmission lines (Fig. 2). In the model, we have not accounted for the substrate loss. The coupled-mode transmission-line equations can now be written as

$$-\begin{bmatrix} \frac{\partial v_1}{\partial x} \\ \frac{\partial v_2}{\partial x} \end{bmatrix} = \begin{bmatrix} R_1 + j\omega L_{11} & j\omega L_{12} \\ j\omega L_{12} & R_2 + j\omega L_{22} \end{bmatrix} \begin{bmatrix} i_1 \\ -i_2 \end{bmatrix} \quad (1)$$

$$-\begin{bmatrix} \frac{\partial i_1}{\partial x} \\ -\frac{\partial i_2}{\partial x} \end{bmatrix} = \begin{bmatrix} g + j\omega(C_{10} + C_{12}) & -(g + j\omega C_{12}) \\ -(g + j\omega C_{12}) & g + j\omega(C_{20} + C_{12}) \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} \quad (2)$$

where the notations are specified in Fig. 2.

Once the line parameters given by expressions (1) and (2) are identified, the two-port  $[Z]$ -matrix of the capacitor can be derived [4] in terms of the element values (Fig. 2) from expressions (1) and (2) with the boundary conditions  $i_1(x = l) = 0$  and  $i_2(x = 0) = 0$ . Since this derivation is made in detail in [3] and [4], it will not be repeated here. If  $C_{12}$  per unit width is very high, the total capacitance ( $C_{10} + C_{20}$ ) with respect to ground is that of a microstrip line with the same width as the capacitor. The separation of the total capacitance into  $C_{10}$  and  $C_{20}$  has been carried out following an approximate approach similar to that described in [5]. The expressions for calculating the capacitance and inductance values are given in the Appendix. In practical applications, the top plate is smaller than the bottom plate and may get virtually screened by the bottom plate. So  $C_{10}$  may be quite small compared with  $C_{20}$ . We will tabulate both the calculated and the optimized values of these elements. In calculating the element values, the

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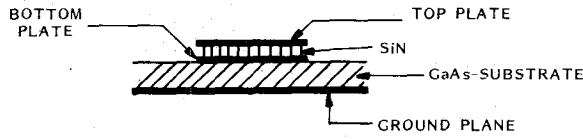


Fig. 1. MIM capacitor on GaAs substrate.

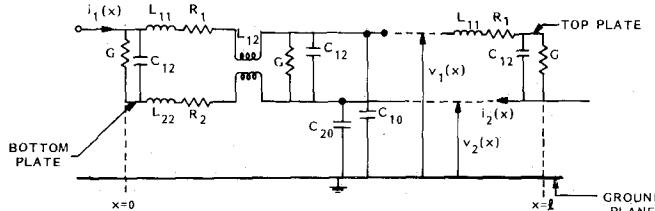


Fig. 2. Distributed model of MIM capacitor.  $L_{11}$ : inductance/unit length of the top plate;  $L_{22}$ : inductance/unit length of the bottom plate;  $L_{12}$ : mutual inductance between the plates/unit length of the capacitor;  $R_1$ : loss resistance/unit length of the top plate;  $R_2$ : loss resistance/unit length of the bottom plate;  $G$ : loss conductance of the dielectric/unit length of the capacitor;  $C_{12}$ : capacitance/unit length of the capacitor;  $C_{10}$ : capacitance with respect to ground/unit length of the top plate;  $C_{20}$ : capacitance with respect to ground/unit length of the bottom plate.  $C_{10}$  and  $C_{20}$  are due to the substrate effects.

top and bottom plate dimensions are assumed equal. The inductance values are calculated from the following expression:

$$[L] = \frac{1}{V_{\text{air}}^2} \begin{bmatrix} C_{10} + C_{12} & -C_{12} \\ -C_{12} & C_{20} + C_{12} \end{bmatrix}_{\text{air}}^{-1} \quad (3)$$

where

$$[L] = \begin{bmatrix} L_{11} & L_{12} \\ L_{12} & L_{22} \end{bmatrix}$$

$V_{\text{air}}$  = velocity of light in air, and the element where  $C_{10}$ ,  $C_{12}$ , and  $C_{20}$  are with  $\epsilon_r = 1$ . The element  $L_{12}$  has been introduced in the present model.  $L_{12}$ ,  $L_{11}$ , and  $L_{22}$  are of the same order for  $C_{12} \gg C_{10}/C_{20}$ , which is usually true in case of MIM capacitors.

### III. MEASUREMENT

Two-port  $S$ -parameters have been measured on a few MIM capacitors. We will present the results for two values of capacitors, nominally 2 pf and 4 pf, with two aspect ratios. The size of the capacitor is carefully chosen; it is not so small that it becomes difficult to measure the effect of the substrate, nor is it so big that it becomes difficult to measure low values of  $S_{11}/S_{22}$  without introducing much error. The measured  $S$ -parameters have been carefully deembedded from the test fixture. One capacitor layout is shown in Fig. 3. The bonding pads (100  $\mu\text{m} \times 100 \mu\text{m}$ ) have been used to bond 0.8-mil wire to 50- $\Omega$  lines on alumina substrate. The bonding wire varies in length from 12 mils to 17 mils. In the optimization program, we have let the inductance of the bond wire vary, along with the associated capacitance, with respect to ground, within their accepted range. During optimization, the bond wire inductances were maintained very close to the calculated values. Fig. 4 shows the complete schematic which has been

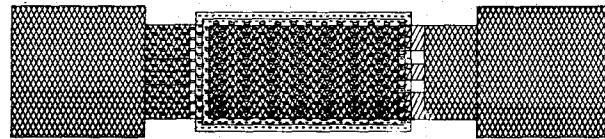


Fig. 3. Capacitor layout.

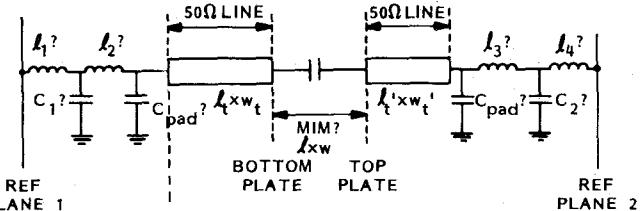


Fig. 4. Schematic of the circuit which has been optimized to fit the measured  $S$ -parameter. The elements shown with "?" are optimized. MIM has the distributed model incorporated in it.  $(l_1 + l_2)$ ,  $(l_3 + l_4)$  are the total inductances for the bond wires.

TABLE I

ELEMENTS	UNITS	CALCULATED	OPTIMIZED
$C_{10}$	pf/m	40	32
$C_{20}$	pf/m	145	157
$C_{12}$	pf/m	31860	29350
$L_{11}$	nH/m	487	460
$L_{22}$	nH/m	486	438
$L_{12}$	nH/m	485	426
$\sigma_{\text{top}}$	mho-m		3.86E7
$\sigma_{\text{bottom}}$	mho-m		3.49E7
$\tan \delta$			.068
$l_1 + l_2$	nH		.26
$C_1$	FF		21
$C_{\text{pad}}$	FF		29
$l_3 + l_4$	nH		.41
$C_2$	FF		30

Capacitor ( $l \times w = 142 \mu\text{m} \times 72 \mu\text{m}$ , top plate), wafer #84.  $l_t \times w_t = 40 \mu\text{m} \times 72 \mu\text{m}$ ;  $l'_t \times w'_t = 50 \mu\text{m} \times 72 \mu\text{m}$ . Bond wire (.8 mil dia.) = 13 mil input, 17 mil output.

Capacitor element values are compared with the calculated values for two different values of caps with two aspect ratios. The calculated values are based on the nominal processing parameters, which are  $\epsilon_{\text{sin}} = 7.0$ , MIM dielectric thickness = 0.14  $\mu\text{m}$ , substrate thickness = 101  $\mu\text{m}$ , substrate dielectric constant = 12.9, capacitor dimension = top-plate dimension, top-plate thickness = 1.5  $\mu\text{m}$ , bottom-plate thickness = 0.5  $\mu\text{m}$ . Also tabulated are the parasitic values with the approximate dimensions for the bonding wire. The various dimension labels are shown in Fig. 4. PECVD was used for SIN deposition.  $\sigma$  is the conductivity for the plates.

optimized. Tables I-IV show the calculated and optimized values of the elements. The measured  $S_{21}$  fits extremely well with the model. Fig. 5 shows the measured and modeled response of the capacitor with the associated parasitics (Fig. 4). The maximum error occurs in the measurement of  $S_{11}/S_{22}$ ; because of their small magnitudes, there was error in deembedding their angles properly. In the present measurement, the main source of uncertainty is the bonding wire. The lengths of the bond

TABLE II

ELEMENTS	UNITS	CALCULATED	OPTIMIZED
$C_{10}$	pf/m	40	22
$C_{20}$	pf/m	200	300
$C_{12}$	pf/m	44692	33000*
$L_{11}$	nH/m	422	400
$L_{22}$	nH/m	421.6	340
$L_{12}$	nH/m	421	360
$\sigma_{top}$	mho-m		3.9E7
$\sigma_{bottom}$	mho-m		3.7E7
$\tan \delta$			.043
$l_1 + l_2$	nH		.33
$C_1$	FF		22
$C_{pad}$	FF		29
$l_3 + l_4$	nH		.36
$C_2$	FF		43

Capacitor ( $l \times w = 101 \mu\text{m} \times 101 \mu\text{m}$ , top plate), wafer #85.  $l_t \times w_t = 60 \mu\text{m} \times 72 \mu\text{m}$ ;  $l'_t \times w'_t = 57 \mu\text{m} \times 72 \mu\text{m}$ . Bond wire (.8 mil dia.)  $\approx 16$  mils.

See footnote on capacitor element values in Table I.

\*It was found to have a thicker dielectric ( $\sim 0.17 \mu\text{m}$  instead of nominal  $0.14 \mu\text{m}$ ).

TABLE III

ELEMENTS	UNITS	CALCULATED	OPTIMIZED
$C_{10}$	pf/m	40	25
$C_{20}$	pf/m	145	180
$C_{12}$	pf/m	31860	29300
$L_{11}$	nH/m	487	495
$L_{22}$	nH/m	486	434
$L_{12}$	nH/m	485	425
$\sigma_{top}$	mho-m		4.07E7
$\sigma_{bottom}$	mho-m		3.5E7
$\tan \delta$			.036
$l_1 + l_2$	nH		.31
$C_1$	FF		28
$C_{pad}$	FF		29
$l_3 + l_4$	nH		.27
$C_2$	FF		26

Capacitor ( $l \times w = 72 \mu\text{m} \times 72 \mu\text{m}$ , top plate), wafer #84.  $l_t \times w_t = 84 \mu\text{m} \times 72 \mu\text{m}$ ;  $l'_t \times w'_t = 85 \mu\text{m} \times 72 \mu\text{m}$ . Bond wire (.8 mil dia.)  $\approx 14$  mils.

See footnote on capacitor element values in Table I.

wires were measured carefully within an accuracy of  $\pm 1$  mil and then their inductances were calculated using the published expressions [6]. The inductance values were also calculated by treating these bonding wires as transmission lines with an average height of 5 mils above the ground. Both these calculations showed very good agreement. The associated capacitances,  $C_1$  and  $C_2$  in Fig. 4, include the open-ended capacitance of the microstrip. The bonding

TABLE IV

ELEMENTS	UNITS	CALCULATED	OPTIMIZED
$C_{10}$	pf/m	41	32
$C_{20}$	pf/m	119	133
$C_{12}$	pf/m	22567	21100
$L_{11}$	nH/m	555	580
$L_{22}$	nH/m	554	490
$L_{12}$	nH/m	553	481
$\sigma_{top}$	mho-m		3.8E7
$\sigma_{bottom}$	mho-m		3.5E7
$\tan \delta$			.044
$l_1 + l_2$	nH		.32
$C_1$	FF		29
$C_{pad}$	FF		29
$l_3 + l_4$	nH		.26
$C_2$	FF		24

Capacitor ( $l \times w = 102 \mu\text{m} \times 51 \mu\text{m}$ , top plate), wafer #84.  $l_t \times w_t = 74 \mu\text{m} \times 72 \mu\text{m}$ ;  $l'_t \times w'_t = 78 \mu\text{m} \times 72 \mu\text{m}$ . Bond wire (.8 mil dia.)  $\approx 14$  mils.

See footnote on capacitor element values in Table I.

pad capacitance  $C_{pad}$  was maintained the same for all the capacitor models. One can further approximate the capacitance associated with the bonding wire itself with the expression

$$\frac{1}{\sqrt{LC}} = V_{air}$$

where  $L$  is the inductance/unit length of the bondwire,  $C$  is the capacitance/unit length of the bondwire, and  $V_{air}$  is the velocity of light in air. Fig. 6 shows the comparison between different models: TFC (SUPER-COMPACT<sup>TM</sup>) [7], line-cap-line, and distributed capacitor with optimized elements. The details of the TFC model are not known to the author. The response of the TFC model takes into account the new values of the capacitance density and the loss tangent as found by fitting the distributed model with the measured data. The response is plotted for two types of capacitors. The line-cap-line model, which is frequently used, consists of a transmission line half the length of the capacitor (used in the TFC model), a capacitor (the value and loss tangent of which are the same as those in TFC), and another transmission line half the length of the capacitor, the width of the line being that used in TFC. Note that one of the capacitors (width =  $72 \mu\text{m}$ , length =  $142 \mu\text{m}$ ) has the same width as that of a  $50\Omega$  line on 4-mil GaAs substrate. So in the limit  $C_{12}$  per unit width  $\rightarrow \infty$  or, for reasonably higher capacitance density, the capacitor should look like a through  $50\Omega$  line at high frequency. The TFC model response (Fig. 6(b)), shows a series inductance of around 7 GHz, whereas the distributed model response approaches a through  $50\Omega$  line response. For the capacitor with higher capacitance density, the optimized model response and the line-cap-line model response look almost identical, because  $(C_{10} + C_{20})$  ap-

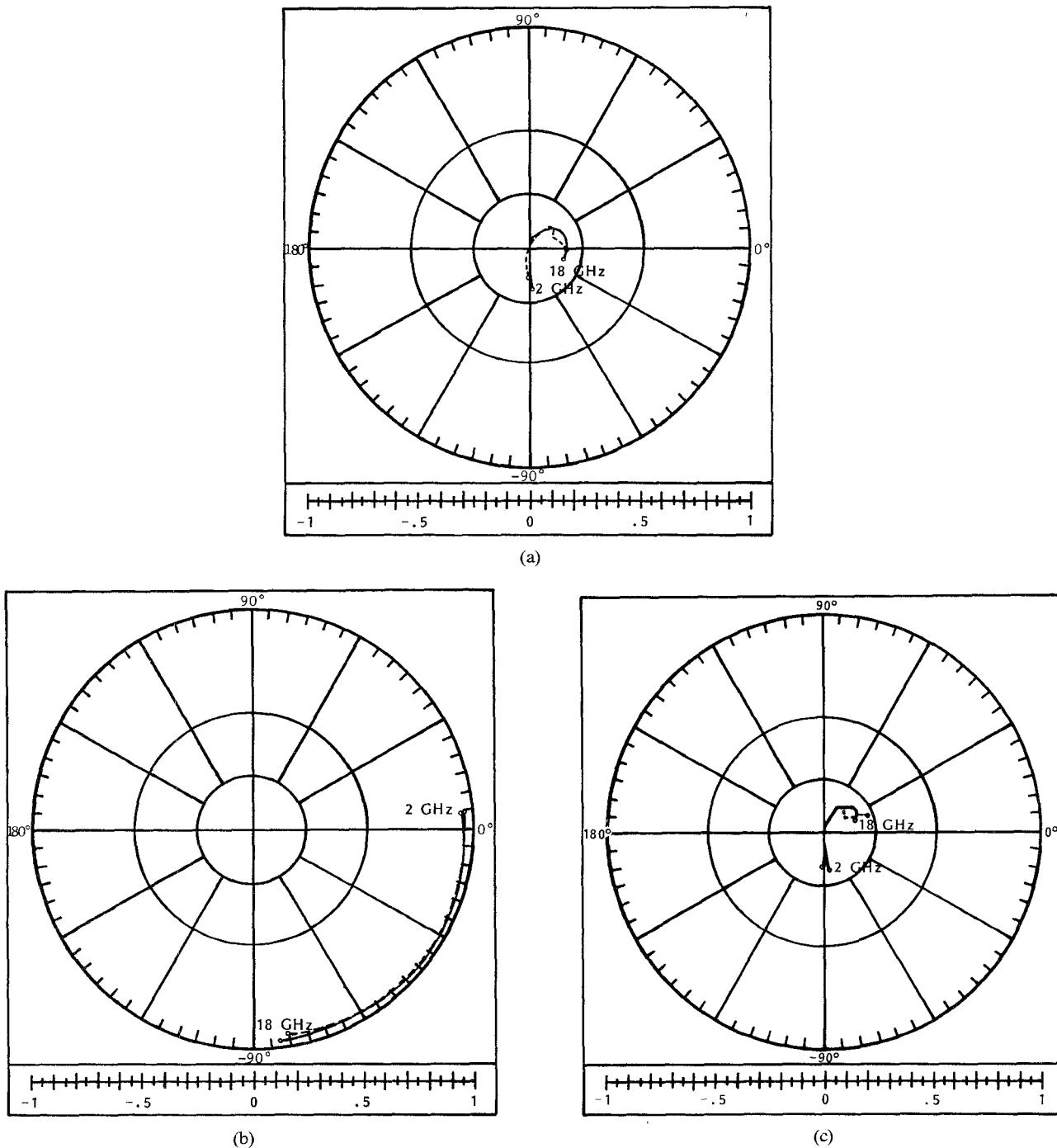


Fig. 5. Measured (----) and modeled (—) data of a capacitor ( $101 \mu\text{m} \times 101 \mu\text{m}$ , top-plate dimension) are compared on polar charts. Small discrepancies between the measured and modeled data for  $S_{11}$  and  $S_{22}$  are mainly due to the deembedding error that has occurred in the measurement of low values of  $S_{11}$  and  $S_{22}$ . (a)  $S_{11}$ . (b)  $S_{21}$ . (c)  $S_{22}$ .

proaches the capacitance of a single microstrip line with the same width as that of the capacitor. Under lossless conditions and  $C_{12}$  per unit width  $\rightarrow \infty$ , the line-cap-line model and the distributed model are identical irrespective of the aspect ratio of the capacitor. These two responses deviate as the capacitance density decreases. This finding is not very surprising. The response of the TFC model did not seem to tally well with the other two responses. Except in the case of sensitive circuit design, this difference in response may not be very critical.

#### IV. DISCUSSION

We have shown a comparison of the responses of the generally adopted MIM cap models with a simple distributed model of the capacitor. The distributed model of the capacitor is optimized with the two-port measured  $S$ -parameter data. The investigation showed that the line-cap-line model compares very well with the distributed model for high capacitance density. The TFC model does not perform as well. For many practical applications

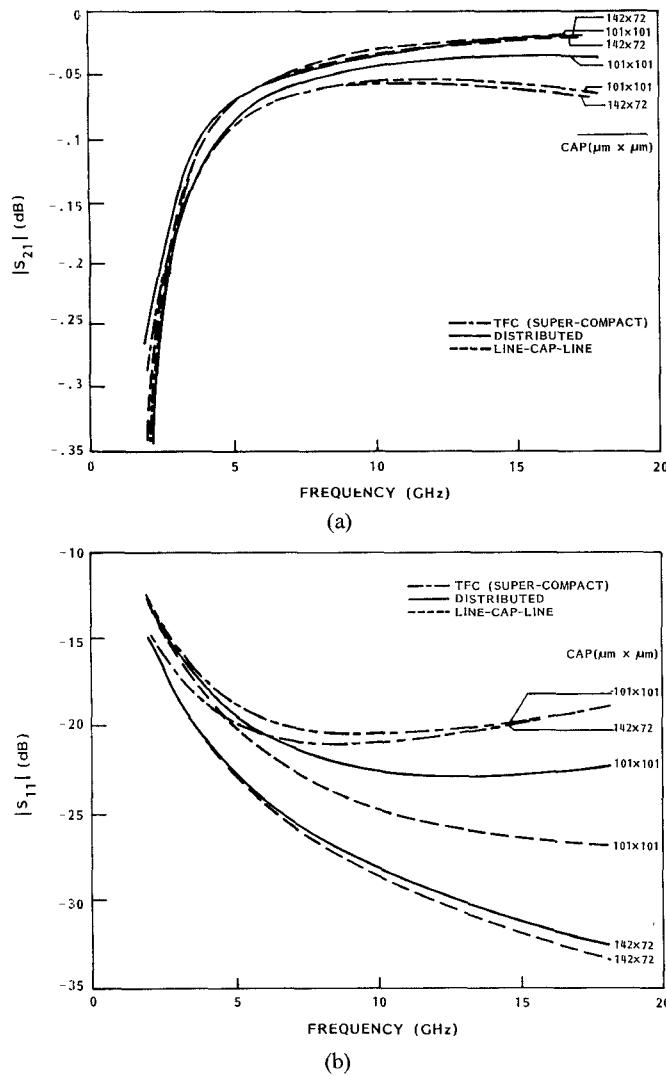


Fig. 6. The magnitudes of  $S_{11}$  and  $S_{21}$  are compared for various models in a  $50\Omega$  system. The capacitor with dimensions  $101\ \mu\text{m} \times 101\ \mu\text{m}$  has capacitance density less than the other one,  $142\ \mu\text{m} \times 72\ \mu\text{m}$ . The line-cap-line model shows a better approximation to the distributed model than the TFC model. (a)  $|S_{21}|$ . (b)  $|S_{11}|$ .

where circuit response is not sensitive to the capacitor response, the TFC model may be adequate. The TFC model with high capacitance density ( $C_{12} \rightarrow \infty$ ) and width equal to that of a  $50\Omega$  line does not behave like a  $50\Omega$  through line. The analysis shows that the line-cap-line model is more accurate than the TFC model, though one has to properly choose the line length to reflect the unsymmetrical property of the capacitor. A comparison between the distributed model response and the line-cap-line model response shows that the line-cap-line model with identical line lengths on either side of the capacitance is quite adequate to represent the MIM capacitor for high capacitance density.

#### APPENDIX

We give the procedure for determining the capacitance and inductance values used in expressions (1) and (2):

$$C_2 = \frac{1}{2} \cdot \left( \frac{Z_{\text{stp}} \cdot V_{\text{air}}}{\sqrt{\epsilon_r}} \right)^{-1} \quad (\text{A1})$$

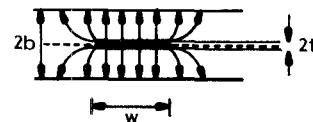


Fig. 7. Stripline used for calculating  $C_2$ .

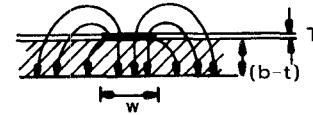


Fig. 8. Microstrip line used for calculating  $C_{\text{tot}}$ .

where

$C_2$  half the capacitance between the stripline and the ground plane (Fig. 7),  
 $Z_{\text{stp}}$  characteristic impedance of the stripline shown in Fig. 7,  
 $V_{\text{air}}$  velocity of light in air,  
 $\epsilon_r$  relative dielectric constant of the medium (for GaAs  $\epsilon_r = 12.9$ ),  
 $t$  thickness of the bottom plate,  
 $b - t$  thickness of the substrate to be used for MIM.

$$C_{\text{tot}} = \left( \frac{Z_{\text{mis}} \cdot V_{\text{air}}}{\sqrt{\epsilon_{\text{eff}}}} \right)^{-1} \quad (\text{A2})$$

where

$C_{\text{tot}}$  total capacitance of the microstrip line of thickness  $T$ , top and bottom plates combined (Fig. 8),  
 $Z_{\text{mis}}$  characteristic microstrip impedance (Fig. 8),  
 $\epsilon_{\text{eff}}$  effective dielectric constant.

$$C_{\text{par}} = \epsilon_0 \epsilon_r \cdot \frac{W}{(b - t)} \quad (\text{A3})$$

where  $C_{\text{par}}$  is the parallel-plate capacitance between the microstrip line and the ground plane.

$$C_{20} = C_{\text{par}} + (C_2 - C_{\text{par}}) \cdot \frac{\epsilon_{\text{eff}}}{\epsilon_r} \quad (\text{A4})$$

where  $C_{20}$  is the bottom-plate capacitance of the MIM.

$$C_{10} = C_{\text{tot}} - C_{20} \quad (\text{A5})$$

where  $C_{10}$  is the top-plate capacitance of the MIM.

In order to find the inductances  $L_{11}$ ,  $L_{12}$ , and  $L_{22}$ , all the capacitances, (A1)–(A5), are calculated with air as the dielectric. Expression (3) in the text is then used to determine the inductance matrix.

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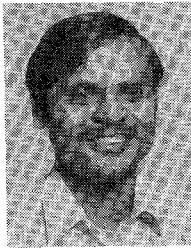
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From 1977 to 1980, he worked with Bharat Electronics Limited, Ghaziabad, India, as an R&D Engineer, developing bipolar power and low-noise amplifier circuits in the *L*-band. His project and thesis work for the M.S. and Ph.D. degrees included variable-gain amplifiers and monolithic phase shifters for *S*-band applications. Since 1984, he has been employed by the General Electric Company, Electronics Laboratory, Syracuse, NY. His present activities are mainly in the microwave monolithic circuit area, involving RF circuits, device physics, and measurement techniques.